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| Year | Semester | | | | Branch | | | | Section | | | |
| Staff Name:M Krishna Chennnakesava Rao | III | II | | | | CSE | | | | All | | | |
| Faculty Branch: ECE | Subject: MPI- 16CS307 | | | | | | | | | MID – 1I | | | |
| Course Name: B.Tech | Date: 01.03.2019 Time: 11.00 – 12.30 AM | | | | | | | | | | | | |

**I. Answer all questions. Each question carries ONE mark. [10 x 1 = 10]**

1. Status lines S4S3=11, indicates \_\_\_\_\_\_\_\_\_\_\_ segment register is being used for data accessing.
2. Which signal of 8086 when it is active, indicates that the processor is performing memory read cycle.
3. 8086 Interrupt Request signal is a \_\_\_\_ triggered input.
4. If the signal on input is High then what happens to 8086 microprocessor operation.
5. If the logic level on pin is LOW, then processor enters into \_\_\_\_\_ mode.
6. Which of the microprocessors listed below have 32-bit internal data registers?

a)8086 b)80286 c)80386-DX e)80386SX f)80486DX

1. List the differences between 80286 and 80386.
2. What is the maximum memory segment size, when the 80386 is operated in Protected Mode?
3. What data is stored in a 386 descriptor table?
4. The paging unit within the 386’s MMU translates 32-bit \_\_\_\_\_\_\_\_\_ addresses into 32-bit \_\_\_\_\_\_\_\_\_ addresses.

**II. Answer any two questions. [2 x 5 = 10]**

11. Design an interface between 8086 CPU and two chips of 16K X 8 EPROM .Select the starting address of EPROM suitably.

**(OR)**

12. Differentiate I/O mapped I/O and Memory mapped I/O

13. Compare various 80x86 family microprocessors.

**(OR)**

14. Illustrate the Paging mechanism in advanced processors.

**II. Answer any one question. [1 x 10 = 10]**

15. Draw and explain the minimum mode configuration of 8086 system and also explain its write cycle operation with one wait cycle.

**(OR)**

16. a)

16.b) The following 80386 program is run to create a new memory segment with the descriptor byte as shown. Answer the following questions about this program and memory segment.

|  |  |
| --- | --- |
| Descriptor No:2 | |
| Byte 7 | 20 |
| Byte 6 | 47 |
| Byte 5 | 79 |
| Byte 4 | 00 |
| Byte 3 | 00 |
| Byte 2 | 00 |
| Byte 1 | FF |
| Byte 0 | FF |

1. Is a global or local descriptor?
2. What is the 32-bit base address of this table?
3. Which descriptor is identified?
4. What is the starting and ending address of the segment?
5. How large is the memory segment?
6. What is the descriptor privilege level?
7. Is the segment Read only or Read Write

MOV AX, 0005H

LLDT AX

MOV AX, 0017H

MOV CS, AX

**Blue print distribution:**

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| **Level** | **Question Nos** | **Total Marks** |
| Remembering |  |  |
| Understanding |  |  |
| Application |  |  |
| Analyzing |  |  |
| Evaluating |  |  |
| Creating |  |  |

**CIRCULAR**

All the Lead faculty members handling B.Tech I, II, & III Year coursework are requested to submit two sets of Mid – I question papers to midqp\_de@vignan.ac.in on or before **20.02.2019**. The question paper model is enclosed.

While sending the mail, mention branch name and subject code in “subject” part of mail. Example: IT & 16CS306.

The title of the attachment should be “subject code\_set1”.

For example 16CS102\_set1.doc

16CS102\_set2.doc

**Note: Use University official mail\_id to send question papers.**